

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	20268	capacitor same transistor same well	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/19 13:14
L2	417	1 same (barrier or shield)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/19 13:15
L3	14146	capacitor with transistor same well	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/19 13:14
L4	228	3 same (barrier or shield)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/19 13:38
L5	87	4 not memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/19 13:38
S13	6889	(257/296,300,368,532).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/12 11:28
S14	29	S13 and transceiver	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/12 13:07
S15	6492	barrier with capacitor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/18 14:19
S16	15	S15 same transceiver	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/18 14:19
S17	87	S15 and transceiver	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/12 13:12

S18	679	S15 and analog	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/12 13:15
S19	149	S15 same analog	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/18 14:25
S20	473	S15 and analog same digital	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/12 13:15
S21	99	S19 same digital	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/12 13:18
S22	3216	metal fill	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/12 13:18
S23	42	S15 and S22	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/12 13:18
S24	1485680	"%" percent percentage	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 13:25
S25	33544	S24 near3 (metal metalization)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 13:26
S26	56	S15 and S25	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 15:21
S27	92	S21 and well	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 15:22

S28	93	(well region) and S21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 15:22
S29	2	(well region) and S21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/12 15:23
S30	30151	(n well) or (p well)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/12 15:23
S31	2	S21 and S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/12 15:24
S32	254	S15 and S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/18 14:26
S33	14	S15 same S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/12 15:24
S34	9694	barrier with transistor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/12 15:30
S35	106	S30 same S34	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/18 14:10
S36	2	"5654984".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/18 14:10

S37	24	("3187260" "3201714" "3290651" "3693114" "3771069" "3909821" "4086534" "4425663" "4493092" "4504793" "4580239" "4697166" "4775864" "4843339" "4875223" "5033062" "5057847" "5083136" "5095291" "5105441" "5384808").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/01/18 14:11
S38	72	("5654984").URPN.	USPAT	ADJ	ON	2006/01/18 14:11
S39	3657	shield with capacitor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/18 14:19
S40	25	S39 same transceiver	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/18 14:19
S41	58	S39 same analog	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/18 14:25
S42	30188	(n well) or (p well)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/18 14:26
S43	53	S39 and S42	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/18 14:26
S44	1188	clock with (barrier or shield)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/19 07:48
S45	30216	(n well) or (p well)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/19 07:32
S46	8	S44 same S45	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/19 07:33

S47	129	S44 same capacitor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/19 07:38
S48	222	clock same block same (barrier or shield)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/19 07:49
S49	75	clock with block with (barrier or shield)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/19 08:07
S50	70	S48 same capacitor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/19 07:53
S51	13	clock with (surrounding or surrounds) with (barrier or shield)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/19 08:40
S52	6894	(257/296,300,368,532).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/19 08:38
S53	3	S52 and S44	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/19 08:38
S54	72	clock same (surrounding or surrounds) same (barrier or shield)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2006/01/19 13:12


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IEEE JNL IEEE Journal or Magazine
 IEE JNL IEE Journal or Magazine
 IEEE CNF IEEE Conference Proceeding
 IEE CNF IEE Conference Proceeding
 IEEE STD IEEE Standard

1. **A clock extraction circuit using passive components-free filter in standard digital**
 Chang, J.J.; Brooke, M.A.
 Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on
 Volume: 2 2000
 Page(s): 261-264 vol.2
 Digital Object Identifier 10.1109/ISCAS.2000.856311
Summary: The necessity of passive components in analog circuit design such as Clock Circuits (CRC) or Phase Locked Loops (PLL) has been a main barrier to overcome especially using a standard digital CMOS process. In addition to lack of support o.....

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2. **Design of multi-valued QMOS pre-decoder**
 Hui Zhang; Uemura, T.; Mazumder, P.; Kyoung-hoon Yang
 Nanotechnology, 2004. 4th IEEE Conference on
 16-19 Aug. 2004
 Page(s): 614- 617
 Digital Object Identifier 10.1109/NANO.2004.1392437
Summary: In this paper, we have proposed two new four-valued pre-decoder circuits stretchable multi-valued decoder frequently used in high-density semiconductor memory are based on resonant tunnelling diode (RTD) having negative.....

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IEEE JNL IEEE Journal or Magazine
 IEE JNL IEE Journal or Magazine
 IEEE CNF IEEE Conference Proceeding
 IEE CNF IEE Conference Proceeding
 IEEE STD IEEE Standard

- Design and performance of an ultra-low phase noise, radar exciter**
 Driscoll, M.M.; Hazzard, A.C.; Opdycke, D.G.
 Frequency Control Symposium, 1994. 48th., Proceedings of the 1994 IEEE Internation
 1-3 Jun 1994
 Page(s): 647-650
 Digital Object Identifier 10.1109/FREQ.1994.398268
Summary: This paper reports on the design and performance of a radar exciter exhibi
 art phase noise characteristics. The exciter provides fully coherent receiver local oscill
 HF, L-band, and X-band as well as requisite, auxilia.....
[AbstractPlus](#) | Full Text: [PDF](#) IEEE CNF
- The core clock system on the next generation Itanium1 microprocessor**
 Anderson, F.E.; Wells, J.S.; Berta, E.Z.
 Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE
 Volume: 1 2002
 Page(s): 146-453 vol.1
 Digital Object Identifier 10.1109/ISSCC.2002.992978
Summary: A PLL generates a high-frequency core clock for a 1GHz processor by mul
 system clock. The clock is distributed across the 19x14 mm² core via a shielded, balai
 the final pulsed gated buffers with <62 ps.....
[AbstractPlus](#) | Full Text: [PDF](#) IEEE CNF
- Noise-constrained interconnect optimization for nanometer technologies**
 Elgamel, M.A.; Tharmalingam, K.S.; Bayoumi, M.A.
 Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Sympo:
 Volume: 5 25-28 May 2003
 Page(s): V-481- V-484 vol.5
 Digital Object Identifier 10.1109/ISCAS.2003.1206323
Summary: Wide, thick wiring, clock frequency in the GHz range will require interconn
 consider inductance and inductive coupling effects on interconnect delay and noise. At
 expressions are preferred because simulation is always expen.....
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